Firmware Development & Pre-silicon Verification with FPGA-based Prototyping

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June 2013

Overview

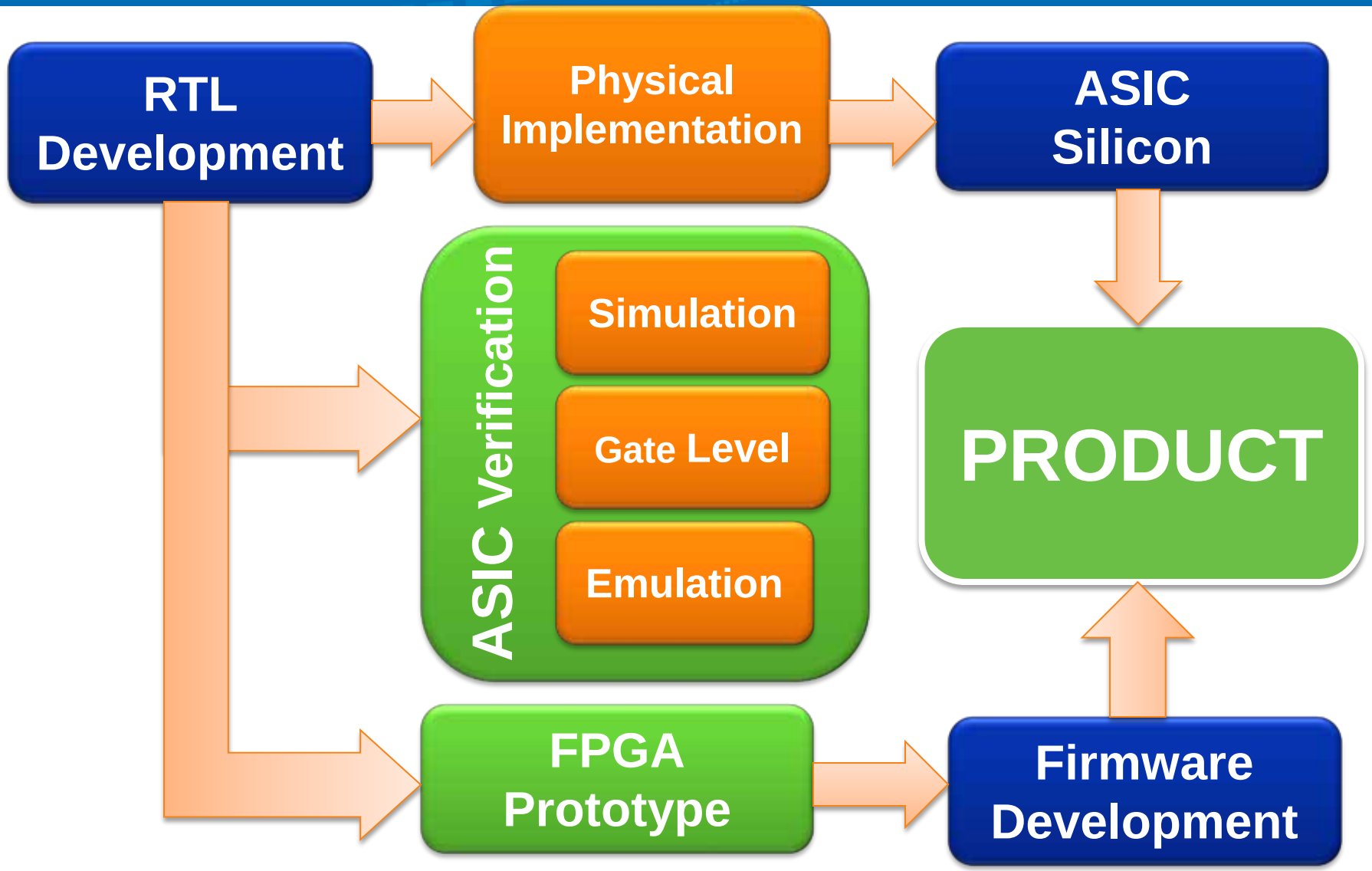
- About sTec
  - sTec designs, develops and manufactures solid state storage solutions based on flash memory and DRAM.
- Smarter solutions for today's IT challenges
  - Database Acceleration
  - Enterprise Applications
  - Cloud Infrastructure
  - Big Data
  - Virtualization/VD

You Already Know Us…
You Just Didn't Know It.

- Powering enterprise IT since 1990
  - Cisco, Dell, EMC, Fujitsu, HDS, HP, IBM, Sun/Oracle, etc.
  - Trusted by critical government agencies around the world
  - First to market with enterprise-class SSDs
  - Expertise in numerous industry segments
- Chances are, we're already in your IT infrastructure
  - Over 14 million SSDs shipped to enterprise environments
  - Broad line of SSD, software, flash and embedded solutions
  - 100+ patents—Solid reputation for performance, reliability, innovation, and support

A global leader with a large installed base

ASIC Verification Platforms
Generic Flow



ASIC Verification Platforms
Characteristics & Primary Use Modes

Gate Level Simulation	• Speed : 1 Hz-10Hz • Debug/Visibility: Full. Large dumps. • Boot, Clock/Reset, Basic Functionality
Simulation (RTL sim)	• Speed : 1KHz-10KHz • Debug/Visibility: Full. • UVM Random, Feature Testing
Emulation (Palladium)	• Speed : 1MHz-3MHz • Debug/Visibility: Full but limited time. • System Scenario, Performance
Prototype (FPGA)	• Speed : 5MHz-50MHz • Debug/Visibility: Very Limited (100-1K signals) • FW Development, Silicon like testing.

Prototype Usage Cases

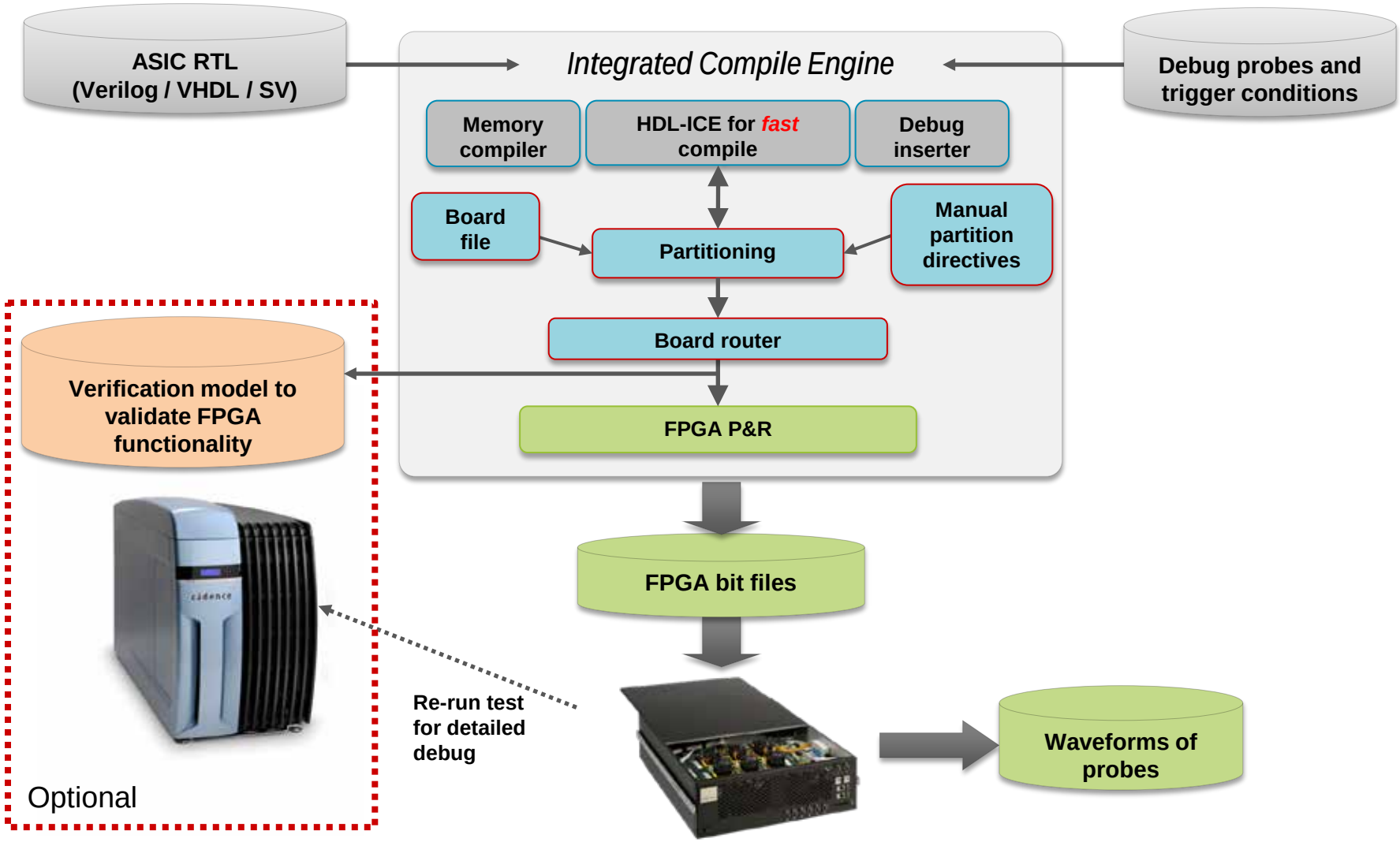
- Firmware Development
  - Provides FW development before Silicon. (Time to Mkt)
  - Allows connectivity with real Peripherals.
  - Approx. 10x+ Faster than Palladium.
  - Ability to use debugger like Lauterbach.
  - Compatibility verification, Driver development.

- Post Silicon Verification Readiness.
  - Prepare Post Silicon test suite before Silicon.
  - Reduces First Pass bring up time by providing a platform to debug tests & environment issues.

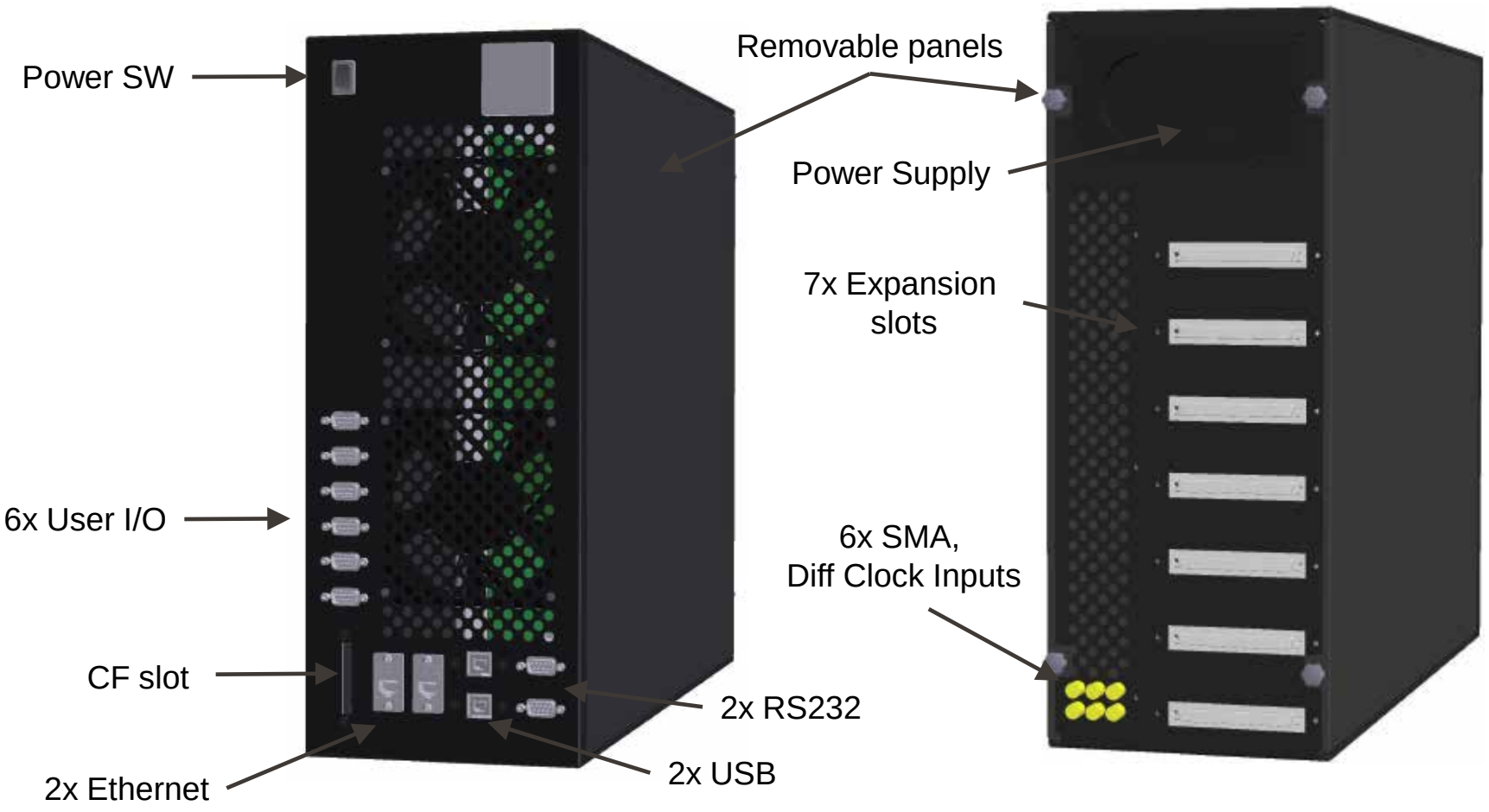
Advantage of RPP Platform

- Doesn’t need additional resource to develop FPGA platform. Share resource/development with Palladium.
- Easy migration from Palladium flow.
  - Automate porting ASIC memories to FPGA Memories.
  - Automate Clock mapping, clock-gate mapping.
  - Automate design partition to multiple FPGA.
  - Only RTL change to fit large DRAMs
- Ability to debug FPGA issues on Palladium.
- Ability to use JTAG debugger like Lauterbach
- Debug flow similar to Palladium.
  - Use simvision gui for waveform debug.

RPP Flow


ASIC RTL
(Verilog / VHDL / SV)
Integrated Compile Engine
Debug probes and trigger conditions
Memory compiler
HDL-ICE for fast compile
Debug inserter
Board file
Partitioning
Manual partition directives
Board router
FPGA P&R
Verification model to validate FPGA functionality
FPGA bit files
Re-run test for detailed debug
Waveforms of probes
Optional

RPP System



RPP Usage Case : Firmware Development

- Compact Flash (CF Slot) contains the FPGA bit file and other information required for build.
- Use Power SW & Reset to re-boot the System.
- Use User I/O for Lauterbach debugger. Download FW image to Internal SRAM/DDR & execute Firmware.
- Use RPP Expansion Slots for Cadence Speed-bridge.
- Use MEG connectors on RPP System for expansion and also connecting to external interfaces.
- Ability to program other User I/O for UART, ARC JTAG and other debug interfaces

RPP Usage Case : Post-silicon Verification Readiness

- This should aid in preparing for Silicon verification Suite before Silicon arrival.
- Connect RPP Box to Linux box with RPP Software.
- Use RPP Software to preload ROM/RAM/DDR memories.
- Run existing verification suite from Palladium in Palladium like environment.
- Modify the setup to run the same test cases using Lauterbach to prepare for Silicon verification.

Questions & Answers