NS115 System Emulation Based on Cadence Palladium XP

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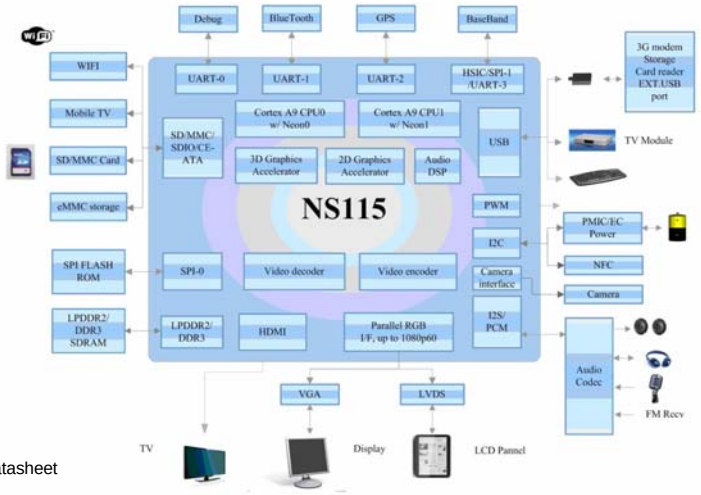
新岸线NUFRONT®

Agenda

- Background and Challenges
- Porting ASIC to Palladium XP
- Software Environment
- Co-Verification and Power Analysis
- Summary

Background and Challenges

- Design Background
  - Verify and emulate the third generation *computer system chip* NS115 with a focus on performance and power with Android applications



Source: nufront NS115 datasheet

Background and Challenges

- Challenges
  - NS115 is a very large and complex design ~12MGates
    - Dual core ARM Cortex-A9 processor
    - Mali400 multi-core 2D/3D graphic processor
    - Dedicated 2D block for hardware acceleration
    - Numerous interfaces and memory subsystems: including LPDDR2, DDR3 memory interface up to 800 Mbps
  - Android system's requirements
    - External storage
    - Multiple screen displays
    - Able to accept data inputs from various sources
    - long starting time for IC simulation
  - Software simulation and FPGA not suitable
    - RTL simulation is too slow for system-level verification
    - Frequently design iterations and lack of full debug visibility not suitable for FPGA

Palladium XP – the solution for emulating NS115

- Performance Improvements
  - About 1000 times faster than software simulation
  - Up to 1.3Mhz real-time frequency
- Resource
  - Able to synthsize and implement the whole chip of 12 million gates
- External Models
  - DDR/eMMc conveniently integrated within
- Real world Interface with SpeedBridge
  - Availability of VGA, UART, SD/MMC, JTAG, USB peripherals

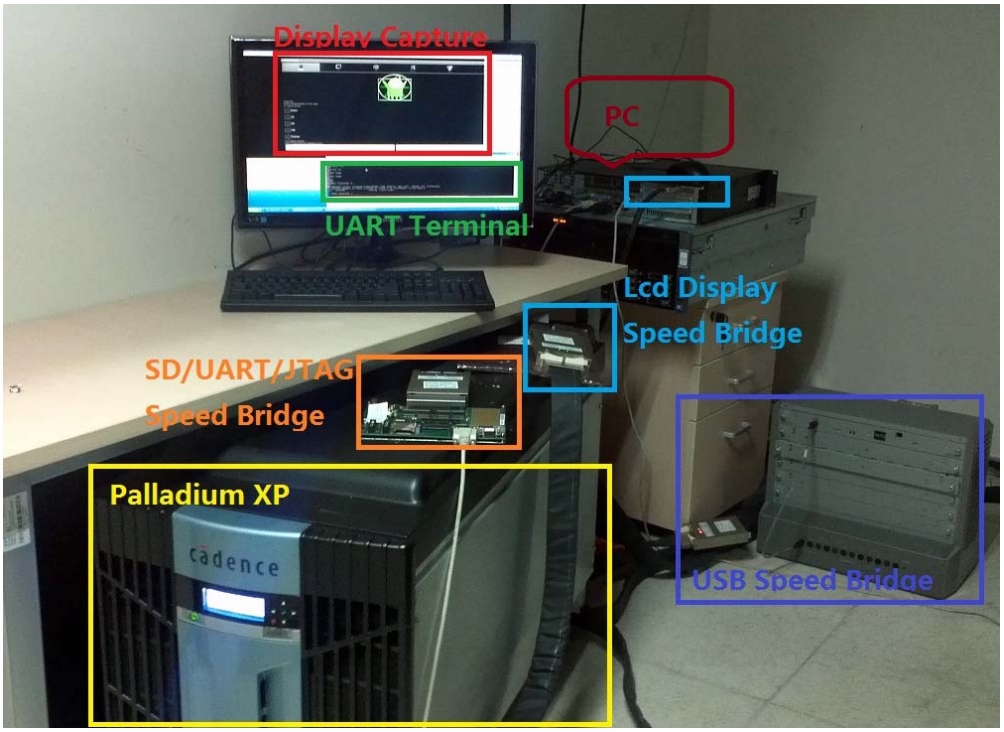
Porting - Synthesis and Compile

- UXE tool and In-Circuit Emulation Mode
- RTL directly ported
- Replace the Un-synthesizable Hard-macro
  - Generate SRAM/ROMs with script
  - DDR PHY and DLL written in Verilog
  - Replace PLLs
- Quick compile time with 1 workstation
  - 40 minutes for a full compile for a 12 million gates design

Porting - Download and run

- XeDebug tool with GUI
  - easy and fast to download and run
- Useful functions of XeDebug
  - Programmable triggers
  - Able to load/dump memory
  - Probe and trace data capture
  - Save/restore
  - Force signals

Palladium XP Emulation Environment for NS115



Software - Android / Linux kernel

- Compile kernel with default bootargs
- Preload kernel image into DDR by memory load function
- Modify ROM boot code to directly jump to kernel

Software - debug methods

- PC registers
  - Probe PC registers to know where CPU executes
  - Trigger PC registers to stop CPU at wanted instruction or function
- Trigger interrupt or exception signals of CPU
- Log system in Linux kernel
  - Dump __log_buf from DDR before UART device and driver are ready
  - Receive logs and input commands through UART SpeedBridge

Software - Linux drivers

- Essential device drivers for Android
  - Interrupt controller
  - Timer
  - Serial port(UART)
  - LCD display controller
  - Sd/MMC/Nandflash controller
- Optional driver for emulation
  - Graphic Processor
  - Video Processor

Software - RAM File System

- Before Android, try RAM file system of busybox
  - small and simple
  - load with kernel image without external storage
  - support basic Linux commands
  - running test cases under linux console
  - can use chroot command to swtich to Android
- About 15 minutes to boot a RAM file system

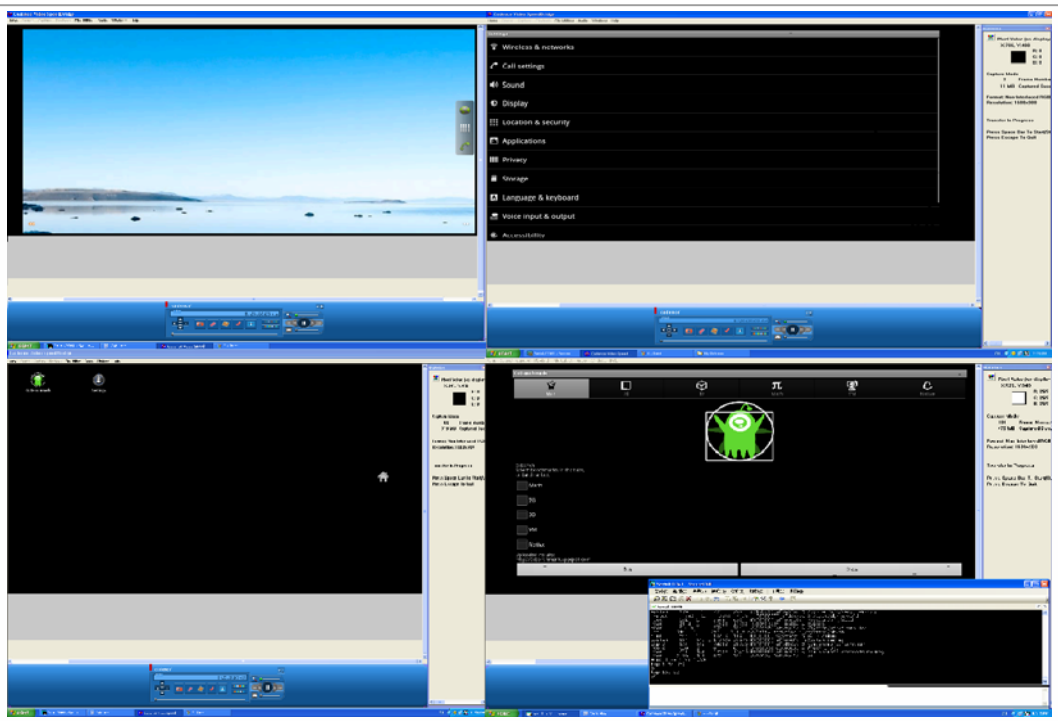
Software - Android (1)

- Refine Android to save boot time
  - Remove unnecessary applications
  - Disable check JNI function
  - Disable unnecessary JAVA classes
  - Remove some unuseful items from init.rc
- Able to boot Android system in about 2 hours vs. a projection of 83 days in a RTL simulator

Software - Android (2)

- Output
  - Capture LCD frames using Video SpeedBridge
- Input
  - Input keyevent, generate key input
  - monkey system, generate touch input
  - am command, start application, service and broadcast intent
- Applications
  - Benchmark applications pre-installed in file system

Emulation Screens

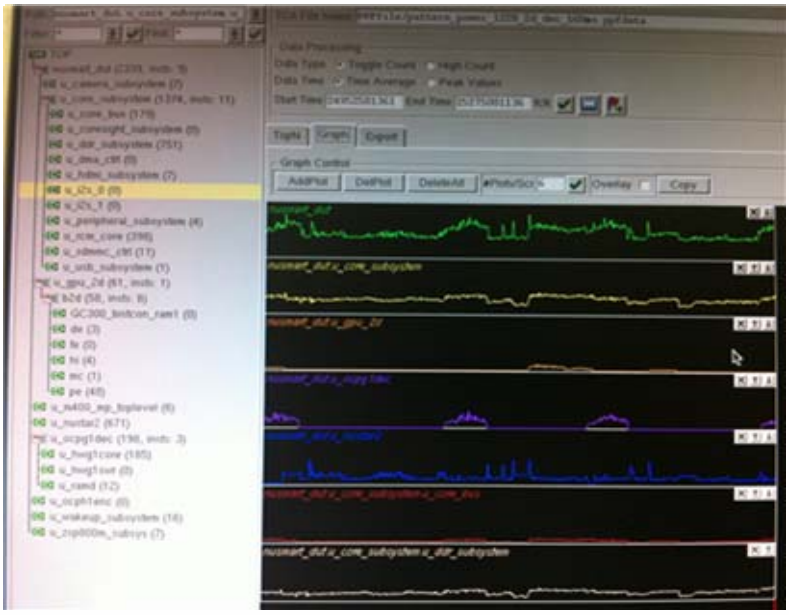


Co-verification using Dynamic Power Analysis (DPA)

- Get data of power peak windows
  - Collect ppfdata of toggle and weighted toggle counts at low resolution
  - Find power peak and zoom into the peak window and re-generate at high resolution
- Power Analysis
  - Generate TCF file for each peak's ppfdata
  - Calculate dynamic power consumption from TCF files, gate level netlist and other libs

Co-verification - DPA Example

- video decode example



Summary

- Benefits of emulating NS115 with Palladium XP
  - Achieved 1000x performance improvement over RTL simulation
  - Enabled early system-level integration and software validation (Android/Linux) with the emulated NS115
  - Correlated power consumption using realistic runtime environments and applications before silicon is available
  - Fast turn around time greatly improve the efficiency of verification

The End

Thanks!

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