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A Deterministic Flow

Combining Virtual Platforms, Emulation, and Hardware Prototypes

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FPGA Hardware Prototypes Provide

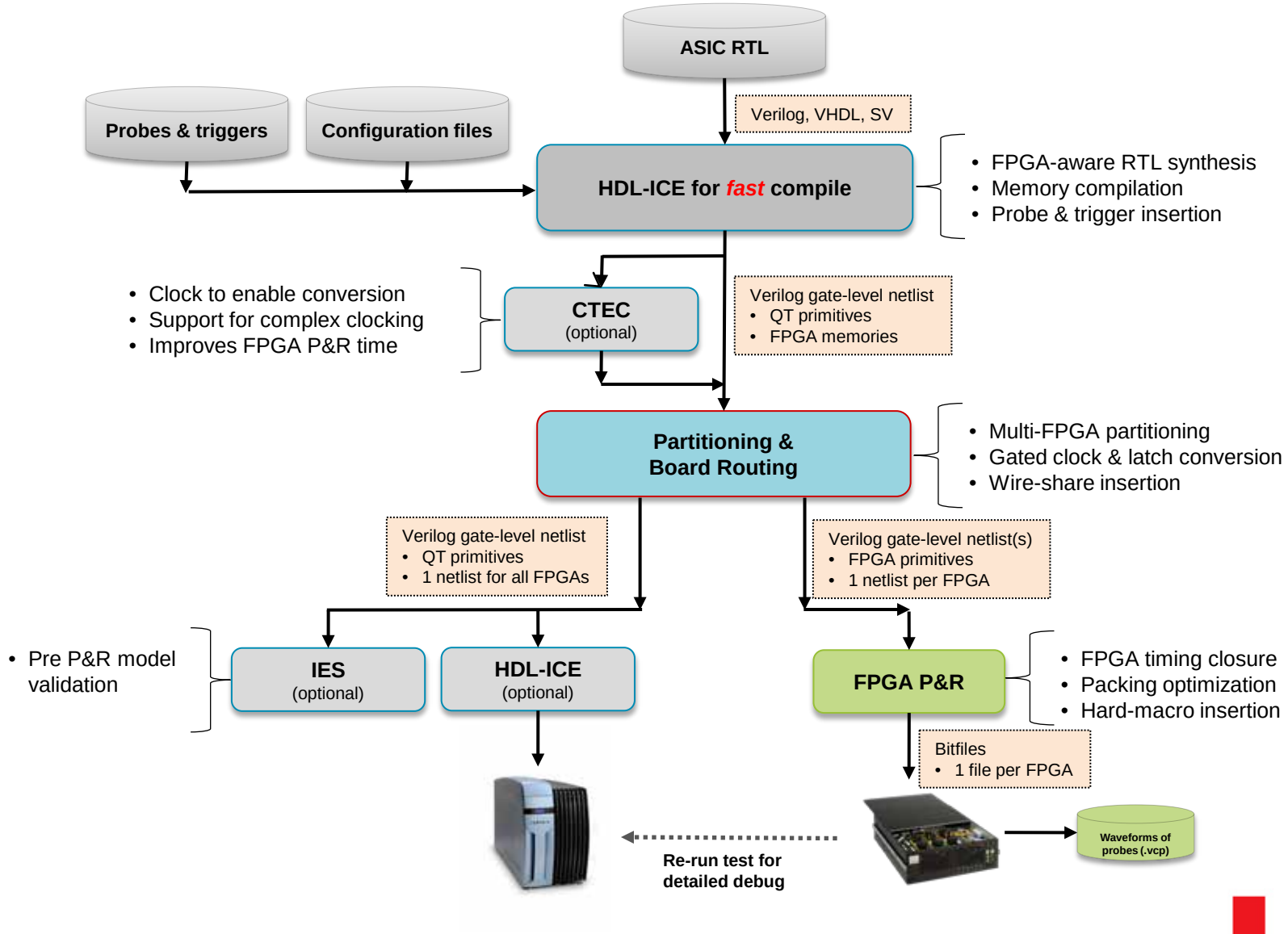
- "Real World" exercise of the System
  - Closest to Chip Behavior
  - Interacts with other Physical Devices in Real-Time
- Hardware/Software integration vehicle
- Detection and debug of subtle system-level "Real Time" problems (Clock Domain Issues)
- Specification verification amongst various compatible products (Plugfest)
- Customer demo

Overcoming Issues for the FPGA Hardware Prototype

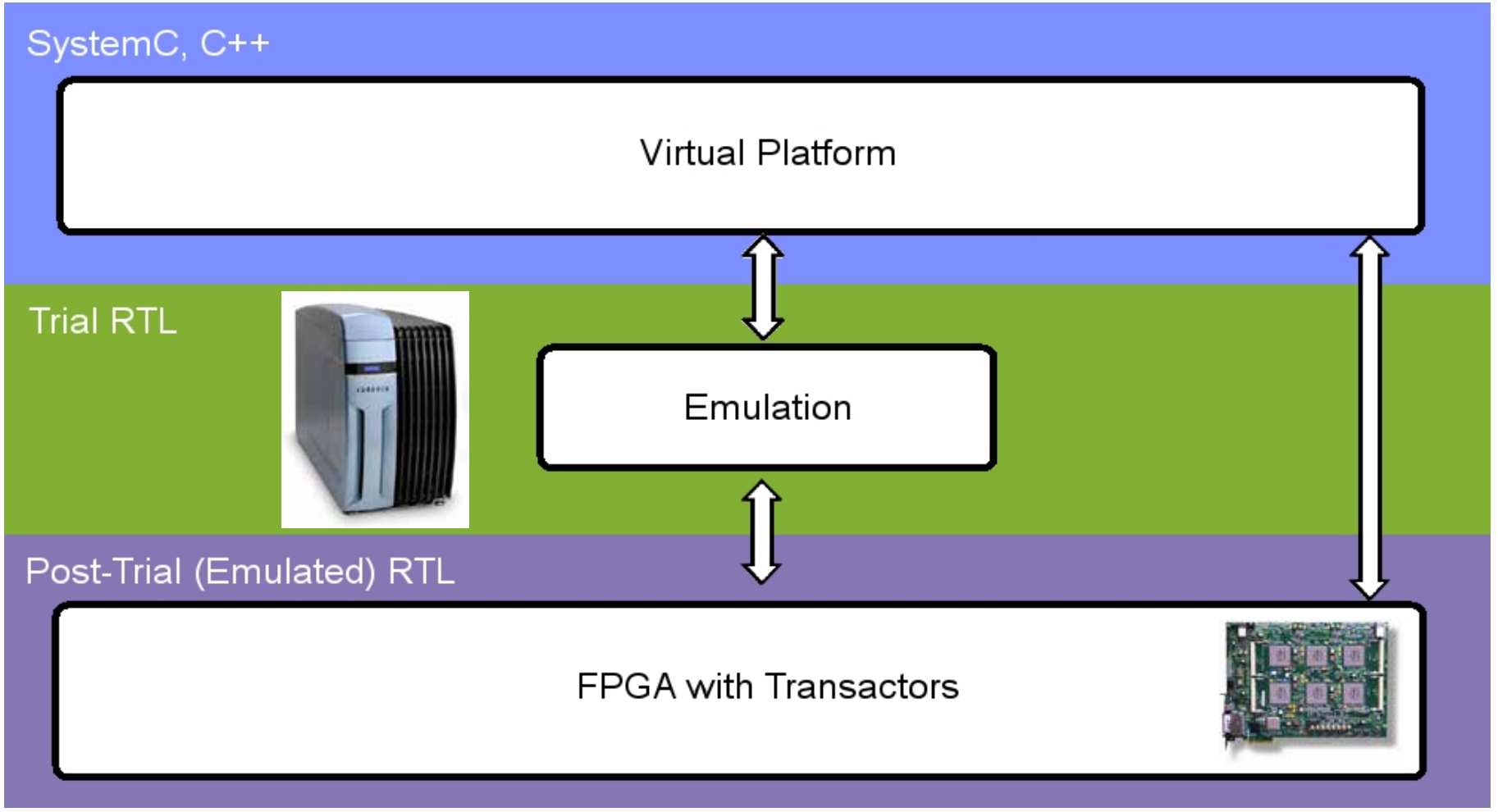
- Must hit a narrow window of opportunity
  - Delays in the development of the prototype reduce effectiveness
- Visibility of internal signals, while improving, remains a challenge
- Quick turnaround of incremental changes improving, but could be better

Multi-FPGA Prototyping Flow

Example: Cadence Rapid Prototyping Platform



Code Staging and Cross Communication



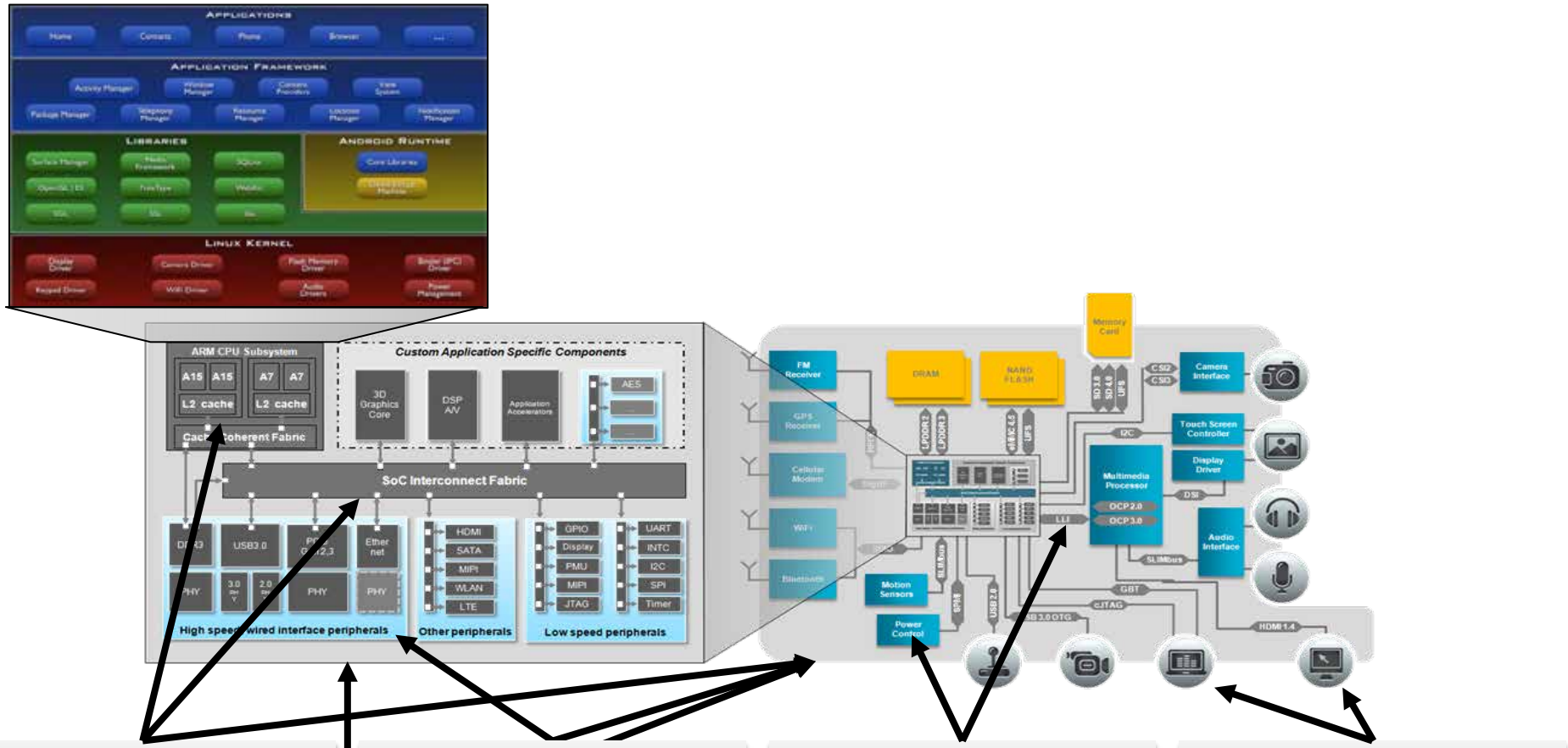
Moving Up the Food-Chain

- In the past, FPGA-specific RTL has been simulated in order to demonstrate basic functionality before downloading bitstreams into the lab.

- For the future, the hope is that this approach could be expanded to include Virtual Platforms and Emulation

Complex Projects Require Many Model Types

Need for optimized reuse of existing IP assets



High-level models
C or SystemC

RTL models
Verilog, VHDL, SystemVerilog

Silicon / hard-macros
Test chip, silicon sample

System and I/Os
Motherboard, PCIE, USB

Instrumentations
Assertions, monitors, checkers

cadence

Virtual Platforms for Emulation and FPGA

§ System-Level Virtual Platform Modeling
- Early HW/SW Integration
  - *Pre-RTL* mutual reinforcement of HW & SW
  - Reduce “Big-Bang” - Integration Surprises
- Architectural Benefits
  - “What-If” scenarios can be tried at high level
  - Bring .pdf “to life” - Reduce EDS/RTL Mismatches

Virtual Platform Goals

§ *Deterministic* Approach – Avoid “surprises” in integration/development

§ Leverage Virtual Platform and Emulation to create FPGA Hardware Prototype

§ Retain the benefits of software simulation
- Cycle-accuracy may suffer, but emulation and the hardware prototype will catch these issues

§ Begin hardware/software integration very early in the development process

§ Hardware/Software Integration should be more transparent when “crossing over” from the virtual world to the hardware prototype
- Emulation/HW Prototypes always result in a “step function” effort
- “Step function” problem should be reduced when the virtual platform is incorporated into the flow

SCE-MI Open Standard for Virtual Platform and FPGA

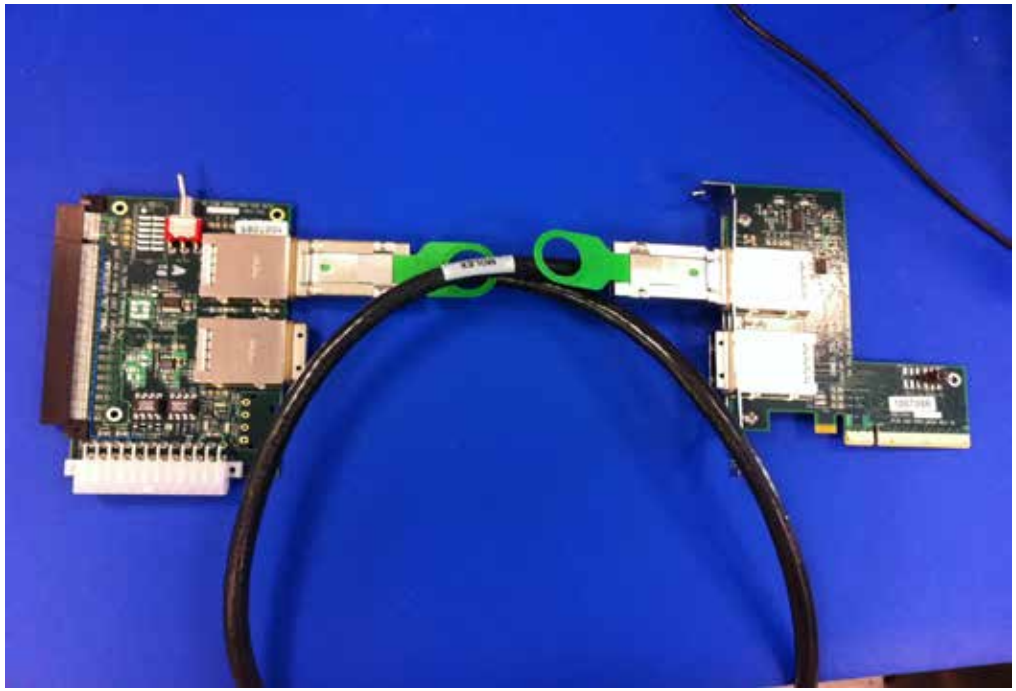
§ Several Serial Protocols could be expected to serve as a vehicle for SCE-MI transactions
  - PCIe
  - Altera SerialLite II
  - Xilinx Aurora
  - SAS/SATA

§ OSCI and Accellera Merge
  - OSCI chair Eric Lish and Accellera chair Shishpal Rawat sign merger documents to create Accellera Systems Initiative*
  - This validates a SCE-MI and SystemC approach to FPGA and Virtual Platform development with a rich and developing set of open standards

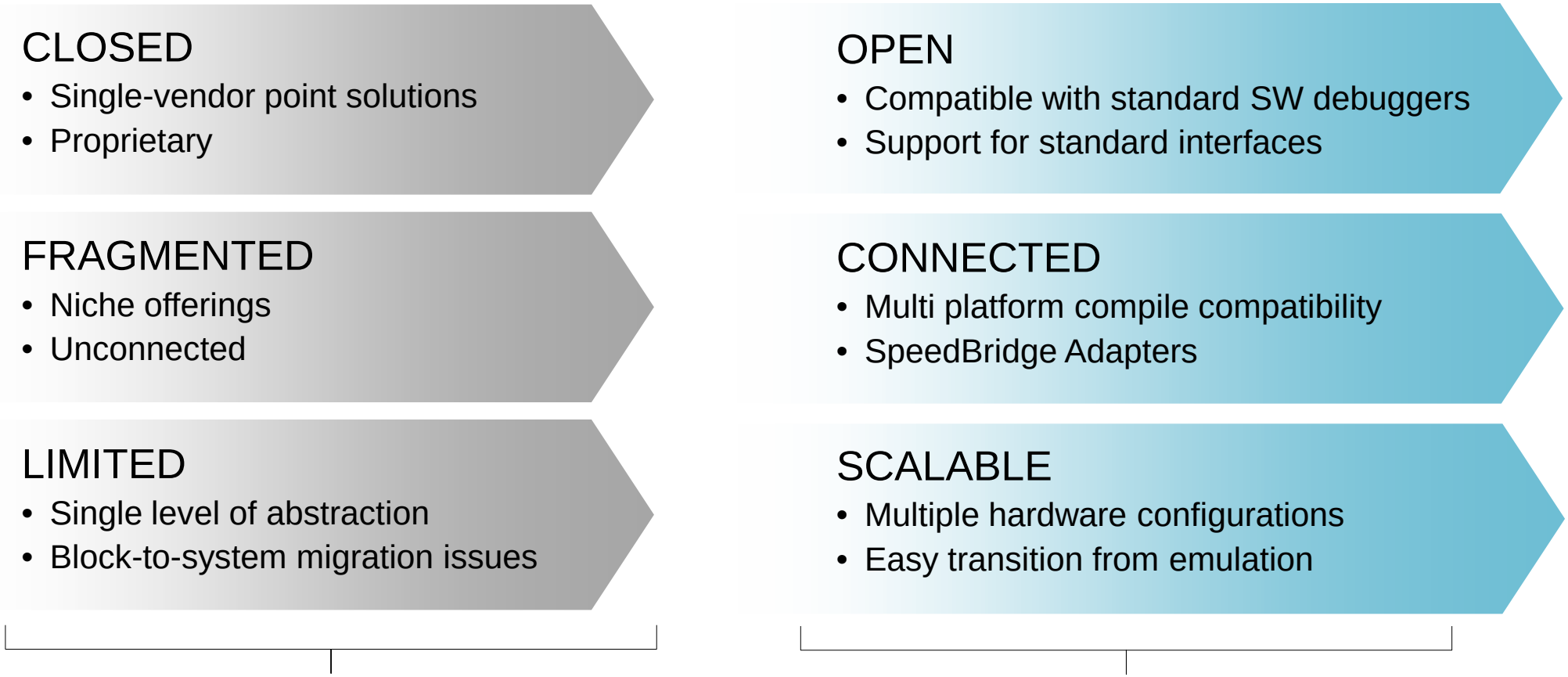
* http://www.accellera.org/about

PCIe Interface Kit

Flexible, scalable 1 – 4 lanes



Evolving System Development And Verification



End-Of-Day Benefits

§Reduced spins of the design

§Much faster chip-evaluation when silicon arrives

- Software ready to go
- Integration/System-Engineering team already up to speed on the device

§Effective widening of the pre-silicon testing window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