

# DEDICATED ASIC DESIGN IS NOW COST EFFECTIVE, DUE TO READILY AVAILABLE PRODUCTION CAPACITY, LOW COST TOOLS AND LOWER PRICED MASKS

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D E E P S U B M I C R O N

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There has never been a better time to explore the advantages of an ASIC, due to the wide availability of low cost design tools and easy access to flexible, mature IC processes. Yet if you read the numerous articles proclaiming the rising cost of semiconductor device development, you would be forgiven for thinking only a smattering of well-funded start-ups, systems companies or device manufacturers could ever afford to take advantage of the many technical and commercial benefits that application Specific Integrated Circuits (ASICs) offer.

## BREAKING THE MYTH

Figures such as a \$25M+ just to buy one mask set, and design costs reaching into the \$100M's seem to mark out ASIC design as a rich person's game. But these figures are only for the leading-edge processes that are cost-justified by large system on chip (SoC) devices in high volume consumer products like PCs and Smartphones. For applications like Internet of Things (IoT), where integration levels are lower, and the need to interface with the "real world" mandates the use of analog circuitry, mature "More than Moore" process technologies are more suitable. Here the costs and risks of using ASIC technology are very different.

Despite the hype about rising costs, ASIC design and production has actually become cheaper for many projects, to the point that many people who used to believe field-programmable gate arrays or microcontrollers coupled with discrete analog devices were their only options are finding out that the dedicated ASIC approach is more cost-effective. The key is to choose the appropriate design tools and more importantly process technology, taking advantage of its maturity to deliver the cost savings and to ensure a wide availability of free or low cost IP. The figure below shows the relative development and production costs for standard IC products, ASICs and reconfigurable parts like FPGAs.

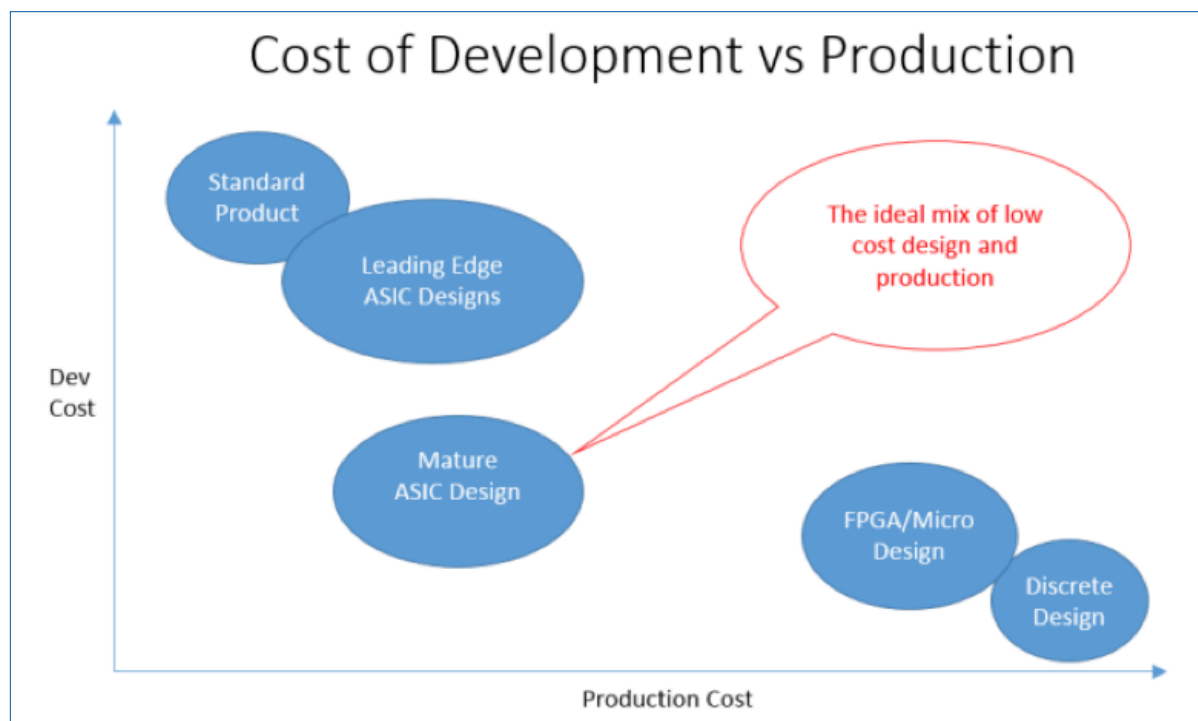


Figure 1: Cost of Development vs Production Chart (Source: Tanner EDA)

## THE ASIC ADVANTAGE

ASIC has a host of other important benefits beyond the low cost of production. ASICs can offer greater performance, lower power, higher voltages, reduced footprint/bill of materials and thus increased reliability. However, perhaps most importantly in this day and age, ASICs offer higher IP security, as an ASIC is far harder to reverse engineer than a microcontroller or FPGA design, where the IP is stored in easy to read memory.

## UPSIDE OF PROCESSES MATURITY

The cost of production in the more mature nodes falls over time as the cost of building the fab is depreciated, with the fab owner only needing to cover the running costs such as staffing and materials. A technology like the ever popular 0.18um mixed-signal CMOS node has been around since the late 90s, so all facilities and equipment costs are well and truly written off.

As well as production costs, design costs for those working in the mature process nodes have improved, particularly for those working on mixed-signal flows. Most of the risk in analog IC design lies in uncertainty. When processes are first rolled out, they offer a moving target to the analog engineer. Key process parameters may shift dramatically from batch to batch as the foundry engineers tweak settings to improve overall yield. This makes it difficult to model analog circuits. However, once the process is optimised the foundry can make available accurate libraries that better reflect the behaviour that engineers will see in the real silicon, reducing design risk. These improvements are realised in foundry specific Process Design Kits or PDKs. These are offered by the foundries, and the more they are used the better they become.

## WIDE AVAILABILITY OF RE-USABLE IP

Moreover, many foundries offering mature mixed-signal processes provide a wide range of pre-characterised IP. The use of such IP blocks is commonplace in the digital world, with world leading UK companies like ARM and Imagination Technologies offering a wide range of functional blocks such as Microcontrollers, many suited to use in these mixed-signal technologies in applications such as Internet of Things. Analog circuit blocks like comparators, operational amplifiers, band gaps, analog to digital and digital to analog converters greatly reduce design time and risk for the designer.

These older processes also offer support for higher voltage operation, which means they are common choices for mixed-signal designs where analog accuracy is important, or the need to work in or control higher voltages are required, such as automotive, industrial control or power management applications.

Some foundries can even tailor their foundry processes to meet specific product or application requirements. Plessey Semiconductors in the UK for example has a unique low power process developed specifically for implanted medical devices such as pacemakers, where battery "life" is not just important, it can be a matter of life or death!

## SHARING THE COSTS

Costs and risks in mask and wafer production can be further reduced by using multi-project wafer (MPW) services from organizations such as EURO PRACTICE IC

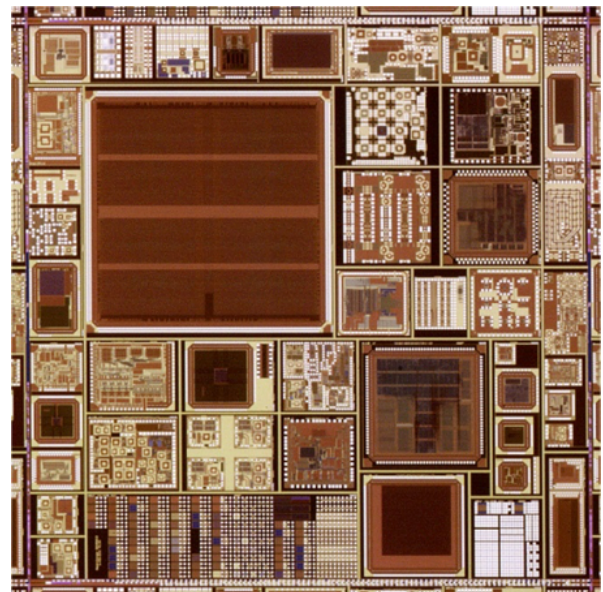


Figure 2: MPW Reticle (Source: MOSIS)

Manufacturing. Where small quantities of chips are needed for evaluation/qualification, or small production runs, several designs can be incorporated in a single mask set, as shown in the Figure 2 (courtesy of MOSIS). Customers typically order 40 devices for evaluation before going to the expense of a dedicated mask set, but up to 1000 devices of any one design could be produced in a single MPW run. MPW costs are just a fraction of those needed for complete set of dedicated masks and wafers, as customers only pay for the proportion of the wafer that their devices occupy. Most major foundries support multi-project wafer services.

A variation on this theme, offered by XFAB®, to further reduce the cost of production mask sets, is for several process layers to be drawn on the same mask. Figure 3 shows 4 layers on one mask, cutting mask costs by as much as 70%. This is known as Multi-Layer Mask or MLM.

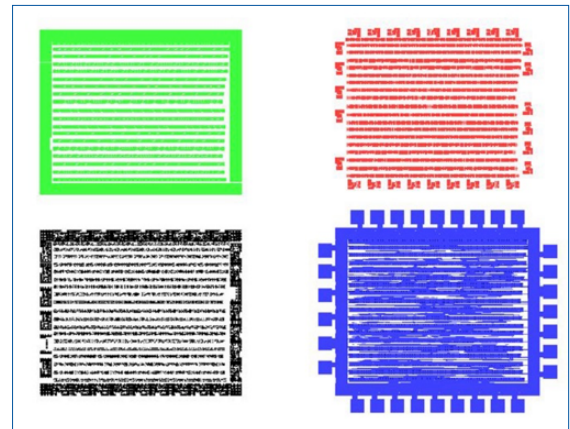


Figure 3: The Multi-Layer Mask (MLM) (Source: XFAB)

It's important to remember that neither older processes nor MPW services inhibit leading-edge analog design. The first single chip Bluetooth transceiver, as shown in Figure 4, was developed in the late 90's by a UK start-up using a 0.35um CMOS process. More recently, when another Cambridge start-up was developing a new generation of communications ASICs to exploit the now free to use unlicensed spectrum previously used by analog TV transmission they turned not to 14nm or even 40nm, but the now mature 90nm process node. The relatively low wafer cost coupled with excellent yield ensured the device offered sufficiently low pricing for the commercially sensitive high volume application, coupled with good analog performance and maturity of process needed to ensure right first time design.

Wide availability of low cost device assembly and test services complete the manufacturing supply chain, ensuring fully functioning packaged, tested chips can be delivered easily and cheaply.

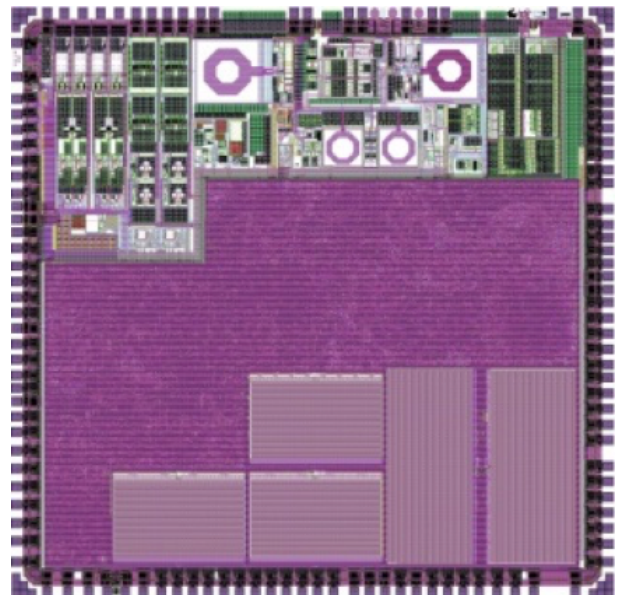


Figure 4: Bluetooth Transceiver (Source: CSR)

## LOW COST DESIGN TOOLS

The use of mature processes brings tool cost down. There is no need to buy expensive leading-edge design tools intended for advanced nanometre SoC design, as they contain many features that are unnecessary for design in the mature nodes. For example, you need a far more complex and thus expensive design tool to perform simulation, layout or verification of a billion gate design in a recently released process node than you do for a relatively simple mixed-signal circuit in a mature process, where the gate count may range in the 10's of 1000's, and most of the analog circuits are IP blocks provided by the foundry and used many times before.

Low cost design tools such as Tanner EDA HiPer Silicon™, which was used extensively in both the above examples, have support for HDL digital design, synthesis and place and route together with support for full custom analog design, allowing engineers to move into mixed-signal chip design on mature processes cost-effectively and easily.

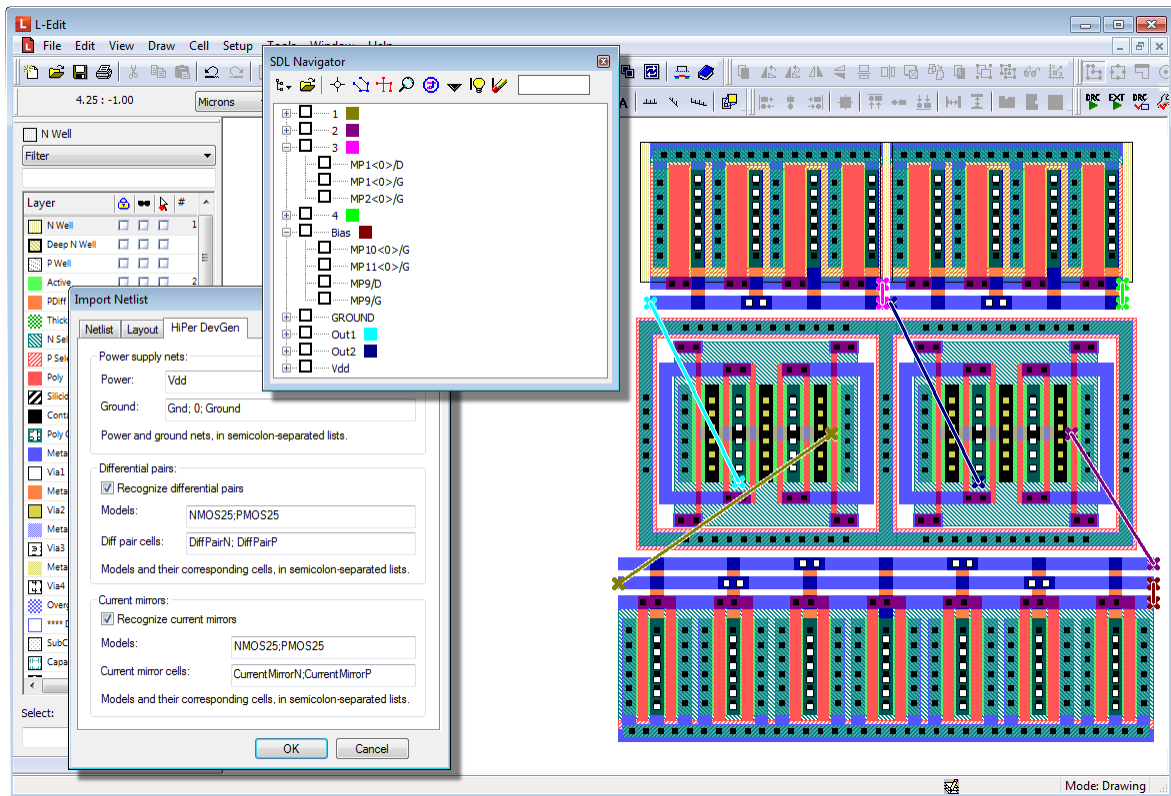


Figure 5: Automated Layout of Operational Amplifier (Source: Tanner EDA)

For the analog side of the design, low cost or even free-to-use open source tools bring many of the benefits that high-end tools offer without unnecessary features and thus cost. Low cost tools are often easier to use because they do not put advanced features in the way. However, this does not mean they lack the functionality or capability of the high-end tools for analog and mixed-signal design. Figure 5 shows the automated layout of an operational amplifier using Tanner EDA HiPer DevGen™ accelerated layout tool.

Another major factor in the choice of design tools is the easy availability of the PDKs needed for accurate and efficient design. This is made easier by the wide adoption in the industry of the emerging interoperable PDK or iPDK standard. iPDKs are developed by most foundries today, and are designed to work with all the major IC design tools. These iPDKs not only contain the basic process related data like simulation models and process layers, but also complex device generation macros known as P-Cells (Parameterised Cells). It used to be that most tool vendors used proprietary languages for their P-Cells and so foundries had to choose which tool vendors to support. Now, with most tool vendors supporting Python as the language used in their P-Cells foundries can support all the major tool vendors with one PDK.

Low cost tools have one further saving on their side. Ongoing support costs are a major feature of high-end tools. To deal with the complexities of setting up and maintaining such leading edge system on chip design flows often demands the support of a dedicated CAD department or the involvement of expensive maintenance contracts. If you are working with a smaller mixed-signal design team, you have to ask yourself whether you need to incur the cost of this type of CAD support, especially when more cost-effective tools are designed to work straight out of the box.

## SUMMARY

For mature processes, IC design is becoming more accessible thanks to the ready availability of production capacity and lower non-recurrent engineering costs made possible by low cost tools and lower-priced processes. There is no need to feel that your only options are FPGAs or discrete Micros with board-level analog circuits. Mature processes allow you to save cost and improve performance by putting the key differentiating elements of your product design into one IC. Custom ICs are no longer the preserve of those companies with deep pockets!

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